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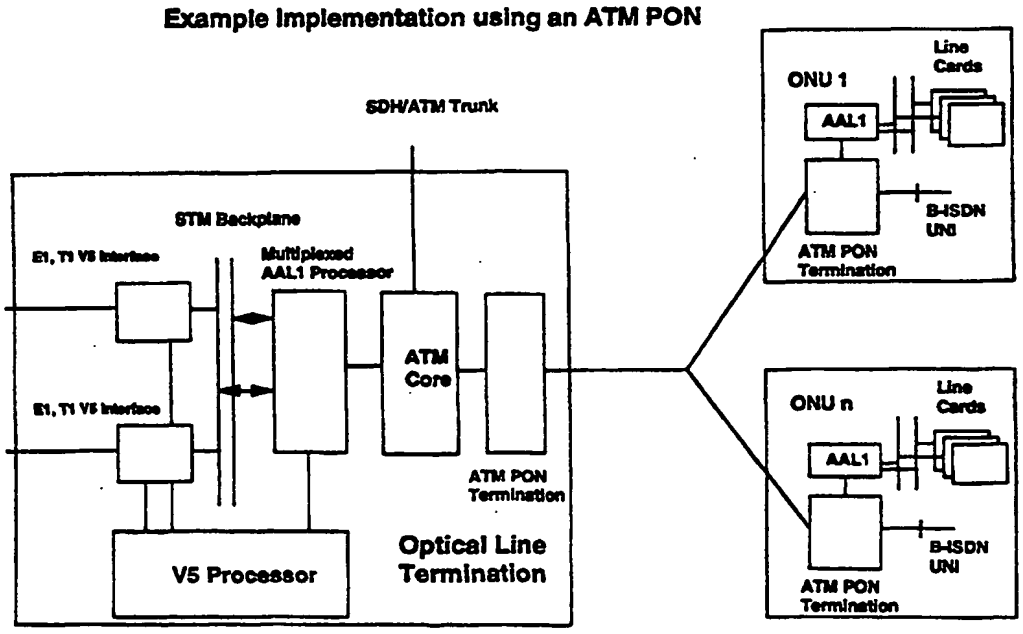

(57) Abstract

An integrated broadband and narrowband access arrangement, includes a muiltiplexed ATM adapter and an ATM core. The ATM core terminates a broadband access system and a narrowband access system whereby to deliver ATM cells to a SDH/ATM trunk or to the adapter. The services comprising the narrowband system are terminated each by a respective adapter providing an individual virtual circuit connection to the multiplexed adapter. The narrowband services within that virtual circuit having permanently assigned time slots whereby to retain time slot sequence integrity throughout the adaptation process.

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ATM ACCESS SYSTEM

This invention relates to digital communications systems and in particular to systems embodying asynchronous transfer mode (ATM) technology.

The asynchronous transfer mode (ATM) technology is a flexible form of transmission which allows any type of service traffic, voice, video or data, to be multiplexed together on to a common means of transmission. In order for this to be realised, the service traffic must first be adapted typically into 53 byte cells comprising 5 byte headers and 48 byte payloads such that the original traffic can be reconstituted at the far end of an ATM network. This form of adaptation is performed in the ATM adaptation layer (AAL). Five types of adaptation layer have been defined. This invention relates to adaptation layer 1 which is used to adapt constant bit rate traffic to the ATM standard.

An ATM exchange may support POTS or ISDN services as well as B-ISDN services. The H320 Video conference standard is a typical user of an nx64Kb/s service, this may well be embedded within a B-ISDN workstation and can also be supported by the N-ISDN. In an ATM exchange with 2Mb/s trunk circuits with independent calls on each 64kb/s channel it is desirable that traffic once adapted to ATM should remain in ATM up to the destination narrowband port. It is further desirable that a physical trunk at e.g. 155Mb/s should be able to carry logical routes to more than one destination as 155Mb/s is generally too large a capacity for trunking within a narrowband service network. If the logical routes are of nx64kb/s where $n \geq 6$ then the cell assembly delay is reduced to the point that echo cancellation is no longer necessary. The cell assembly delay of a single 64kb/s circuit is 6 msec which requires echo cancellation for interworking with the existing narrowband network.

According to the present invention there is provided an asynchronous transfer mode (ATM) processor adapted to terminate a broadband access system and deliver ATM cells to a SDH/ATM trunk on to a multiplexed AAL1 processor.

According to the invention there is further provided an integrated broadband and narrowband access arrangement, including a multiplexed ATM adapter, an ATM core associated with the multiplexed adapter, wherein the ATM core terminates a broadband access system and a narrowband access system whereby to deliver ATM cells to a SDH/ATM trunk or to the adapter, wherein the services comprising the narrowband system are terminated each by a respective adapter providing an individual virtual circuit connection to the multiplexed adapter, the narrowband services within that virtual circuit having permanently assigned timeslots whereby to retain timeslot sequence integrity throughout the adaptation process.

According to another aspect of the invention there is provided a method of tramsmitting traffic in an integrated broadband and narrowband access arrangement comprising a multiplexed ATM adapter and an ATM core associated with the multiplexed adapter, wherein the ATM core terminates a broadband access system and a narrowband access system whereby to deliver ATM cells to a SDH/ATM trunk or to the adapter, the method including terminating the services comprising the narrowband system each by a respective adapter providing an individual virtual circuit connection to the multiplexed adapter, and providing the narrowband services within that virtual circuit with permanently assigned timeslots whereby to retain timeslot sequence integrity throughout the adaptation process.

Our co-pending United Kingdom application No 9410294.4 S D Brueckheimer, R H Mauger 7-6) of even date relates to a flexible implementation of ATM adaptation layer 1 . The present invention relates to the use of a multiplexed AAL1 adapter to enhance a flexible access

system so that it can import both broadband and narrowband services in a flexible manner. In this context narrowband is understood to include services that are provided in a synchronous transfer mode (STM), typically channelled at 64Kbit/sec, and broadband is understood to cover services which are provided by the asynchronous transfer mode (ATM). The bandwidths of the two services may overlap.

An embodiment of the invention will now be described with reference to the accompanying drawings in which:-

Fig. 1 is a schematic diagram of a flexible AAL1 processor.
Fig. 2 is a block schematic diagram of the processor of Fig. 1.
Fig. 3 is a schematic diagram of a multiplexed ATM adapter according to the invention.
Fig. 4 illustrates an implementation of the system of Fig. 3 using an ATM passive optical network; and
Fig. 5 illustrates the interworking of individual AAL1 adapters and the multiplexed adaptater of Fig. 3.

Figs 1 and 2 together provide an illustration of the AAL1 implementation.

In a typical narrowband telecommunications system a common STM bus is available on the backplane of the equipment. This is used as the interface between the equipment which adapts external interfaces such as Analogue or ISDN lines and the equipment which performs the intrinsic function such as switching. An equipment which adapts to an external STM1 system would typically have 2048 64Kb/s channels available on the backplane to the adaptation function. The purpose of the equipment is to allow the adaptation of a number of 64Kb/s channels say 2048 into a number of nx64Kb/s ATM virtual circuits and the readaptation to 64Kb/s channels within the following constraints.

- Any 64Kb/s channels can be associated with any ATM virtual circuit.

- Any group of P 64 Kb/s channels can be assembled together as part or whole of an ATM virtual circuit and will maintain timeslot sequence integrity through the adaptation and transmission processes.

- For conformance to AAL1 standards n is restricted to values from 1 to 30 for proprietary applications n can have any value up to the full capacity of the system.

- The number of ATM virtual circuits m can be any value up to the limit of 1 64 Kb/s circuit per ATM VC i.e. $1 \leq M \leq 2048$ for this example.

The principle of the mechanism is illustrated in figure 1 and the functional block diagram of its implementation is illustrated in figure 2. In both diagrams a process is implied, but not shown, which runs at e.g.125 microsecond intervals and staticises the STM stream on the backplane into an egress frame memory and takes the contents of an Ingress frame memory and distributes this as an STM stream to the backplane. The mechanism is controlled by a chain structure. Each link in the chain is embodied as a combination of two bi-directional pointers and an address in the egress or ingress frame memory, there is one link for each 64 Kb/s channel in each of the egress and ingress chains. Chains are linked to headers and there is one header for each potential nx64Kb/s ATM virtual circuit, headers are embodied by the association of a channel count for control purposes, a VC identity for cell assembly purposes and a bi-directional pointer to the first link of the chain. A chain is assembled for each active ATM virtual circuit and consists of a number of links which use bi-directional pointers to point upwards to the header or previous link and downwards to the next link. Each link contains the address in the frame memory of the required frame sample; links which have not been allocated are formed into a chain which is formed under a special FREE header. Separate egress and ingress chain processes are initiated each 125 microsecond cycle. These process each chain in turn and each link in the

chain in turn and deliver an address to the voice memory and a VPI/VCI to a cell assembly or disassembly process. For the cell assembly process the frame samples are read at each address and change and placed in the next available byte position within the cell payload. Filled cells are assembled with their ATM Header and AAL1 SAT-PDU header and launched into the ATM. A new cell is then generated for that virtual circuit.

For the cell disassembly process cells are unpacked a byte at a time and frame samples are written to the ingress frame memory according to the address delivered by the ingress chain processor, on receipt of an indication from the AAL1 of the boundary of an nx64 Kb/s frame. The cell disassembly process then checks for phase synchronism between egress and ingress functions. The chains are updated under control of a chain update processor under instructions from the system control (not shown). The chain update processor operates a request/grant mechanism with the chain processors to ensure that a chain is not being modified at the same time as it is being processed. If an independent 64 Kb/s channel is being modified then it can be inserted or deleted from any point in the chain. An insertion process uses a link from the FREE chain. A deletion process returns a link to the FREE chain. If a Px64 Kb/s service is being set up then the channels must be inserted in the correct order in consecutive links in the chain.

An embodiment of the invention is illustrated in Figure 3. The core of the system is an ATM processor which is able to terminate a broadband access system and deliver ATM cells to a SDH/ATM trunk or to a multiplexed AAL1 processor as described above. Broadband access systems may be based on ATM PONs fibre/coax hybrid networks or other well known access technologies. Attached to the broadband access system are one or more narrowband access systems which deliver services in a 64 Kb/s channelised mode. The interface between the narrowband access and broadband access is provided by an AAL1 adapter and in particular a nx64 Kb/s structured data transfer variant of AAL1. Narrowband access systems may be PONs, radio or other well

known access technologies. The multiplexed AAL1 processor interfaces to an STM backplane to which are attached adaptation devices to channelised trunk systems such as the 2 Mb/s E1 trunk or the 1.5 Mb/s T1 trunk system. This arrangement provides flexible interworking of circuits within the narrowband access domain and channels within the external channelised trunks, this being achieved by the multiplexed AAL1 system providing an implicit grooming or cross-connection function.

An example implementation of the concept is illustrated in figure 4. This shows an ATM passive optical network (PON) as the broadband access system. The narrowband access system may be a collection of line cards providing narrowband services which are connected to a common STM backplane within the optical network unit (ONU) that houses the ATM PON termination. An AAL1 adapter provides the interface between the STM backplane and the ATM PON termination. The arrangement described herein relates to the interworking between the individual AAL1 adapters in the ONUs and the multiplexed AAL1 adapter in the optical line termination. This interaction is illustrated in Figure 5. Each individual AAL1 adapter in the ONUs has a separate virtual circuit connection to the multiplexed AAL1 adapter in the optical line termination. Within that virtual circuit, narrowband services connected in the ONUs are permanently assigned timeslots within the nx64 Kb/s AAL1 structure. These may be individual 64 Kb/s channels or Px64 Kb/s channels supporting timeslot sequence integrity. The channelised trunks are terminated in the standard manner and their channels are presented in permanently assigned positions on the STM backplane of the optical line termination. The operation of flexible access systems is standardised by two interface standards, the Q interface standard which allows the system to be configured from a network management system and the V 5 interface which in the V 5.2 version allows channels connecting to a switch to be dynamically configured on a per call basis. This is implemented using eg the bearer channel connection protocol in V 5.2.

The multiplexed AAL1 adapter allows any channel within any virtual circuit to be connected to any channel on the backplane either under request from the Q interface or from the V 5.2 interface. It therefore emulates the operation of a cross-connect or a switch which is required in conventional implementations. With reference to figure 1, when a new ONU is configured by operation over the Q interface, then a virtual circuit is configured between the AAL1 adapter in the ONU and the multiplexed AAL1 adapter. This is embodied by establishing a new chain with a link for each configured channel at the ONU. At this point the channels on the channelised trunks have not been assigned so the links in the chain are populated with default addresses in the frame memory such that no connection takes place. As channels are assigned on the V 5 interface whether by the Q interface or the V 5.2 interface, then the default address in the chain links is updated to the real assigned address.

CLAIMS:

1. An integrated broadband and narrowband access arrangement, including a multiplexed ATM adapter, an ATM core associated with the multiplexed adapter, wherein the ATM core terminates a broadband access system and a narrowband access system whereby to deliver ATM cells to a SDH/ATM trunk or to the adapter, wherein the services comprising the narrowband system are terminated each by a respective adapter providing an individual virtual circuit connection to the multiplexed adapter, the narrowband services within that virtual circuit having permanently assigned timeslots whereby to retain timeslot sequence integrity throughout the adaptation process.

2. An integrated broadband and narrowband access arrangement as claimed in claim 1, wherein the narrowband system comprises a set of line cards coupled to a common STM backplane.

3. An integrated broadband and narrowband access arrangement as claimed in claim 2, wherein the multiplexed adapter allows any channel within any virtual circuit to be connected to any channel on the backplane.

4. An integrated broadband and narrowband access arrangement as claimed in claim 2 or 3, wherein the backplane incorporates an ingress and an egress memory, there being means for storing a synchronous transport mode (STM) stream into the egress frame memory, and means for distributing the content of the ingress frame memory as an STM stream.

5. An integrated broadband and narrowband access arrangement as claimed in claim 4, wherein the storing and distribution processes are controlled by a chain structure, each link in the chain comprising two bidirectional pointers and an address in the egress or ingress frame memory, there being one link per channel in each of the egress or ingress chains.

6. A method of tramsmitting traffic in an integrated broadband and narrowband access arrangement comprising a multiplexed ATM adapter and an ATM core associated with the multiplexed adapter, wherein the ATM core terminates a broadband access system and a narrowband access system whereby to deliver ATM cells to a SDH/ATM trunk or to the adapter, the method including terminating the services comprising the narrowband system each by a respective adapter providing an individual virtual circuit connection to the multiplexed adapter, and providing the narrowband services within that virtual circuit with permanently assigned timeslots whereby to retain timeslot sequence integrity throughout the adaptation process.

7. A method as claimed in claim 6, wherein the storing and distribution processes are controlled by a chain structure, each link in the chain comprising two bidirectional pointers and an address in the egress or ingress frame memory, there being one link per channel in each of the egress or ingress chains.

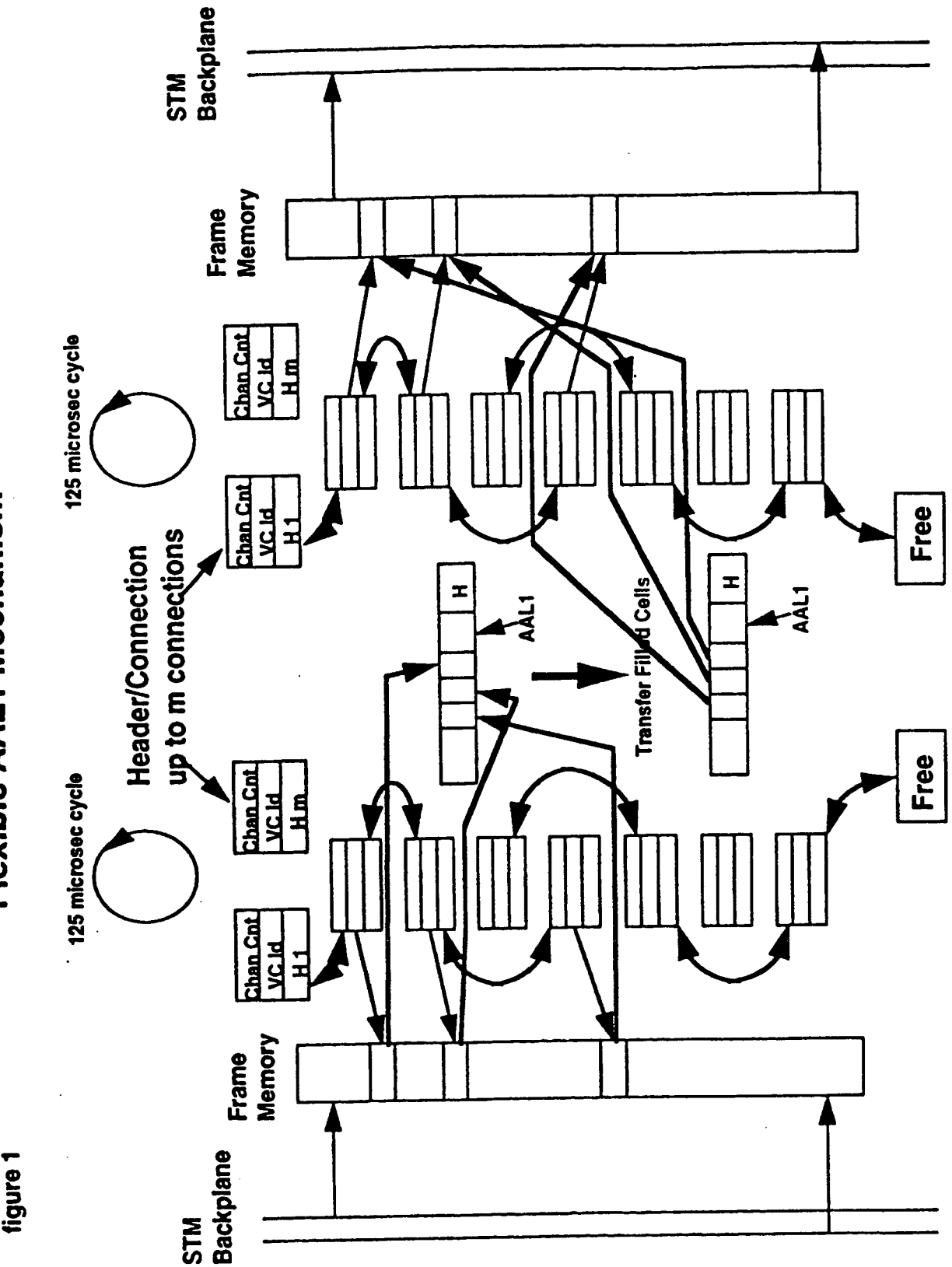

Flexible AAL1 Mechanism
STM Backplane
Frame Memory
125 microsec cycle
Header/Connection up to m connections
Chan Cnt
VC Id
H 1
H m
H
AAL1
Transfer Filled Cells
Free
125 microsec cycle
Frame Memory
STM Backplane

figure 1

Flexible AAL1 Functional Block Diagram

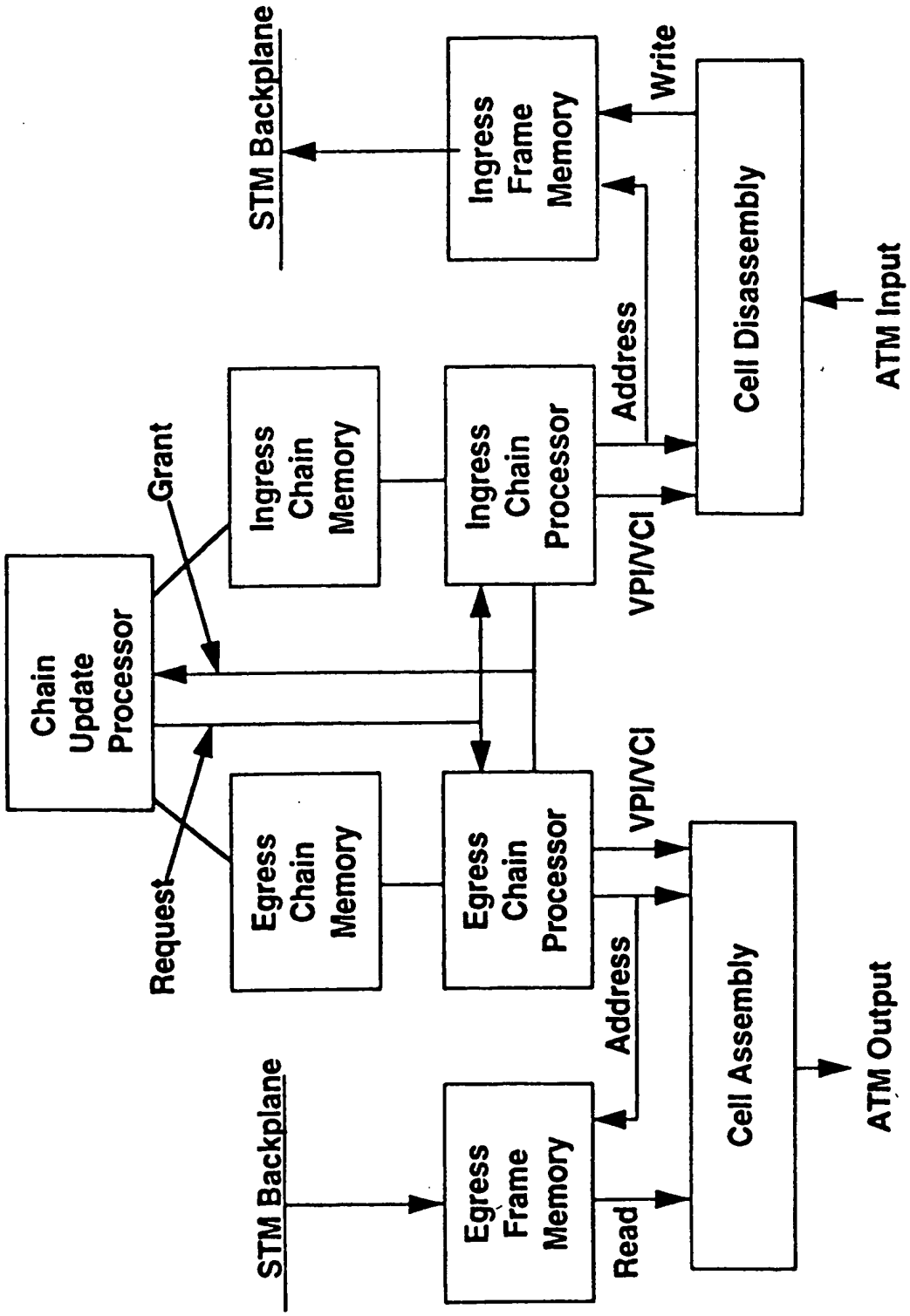
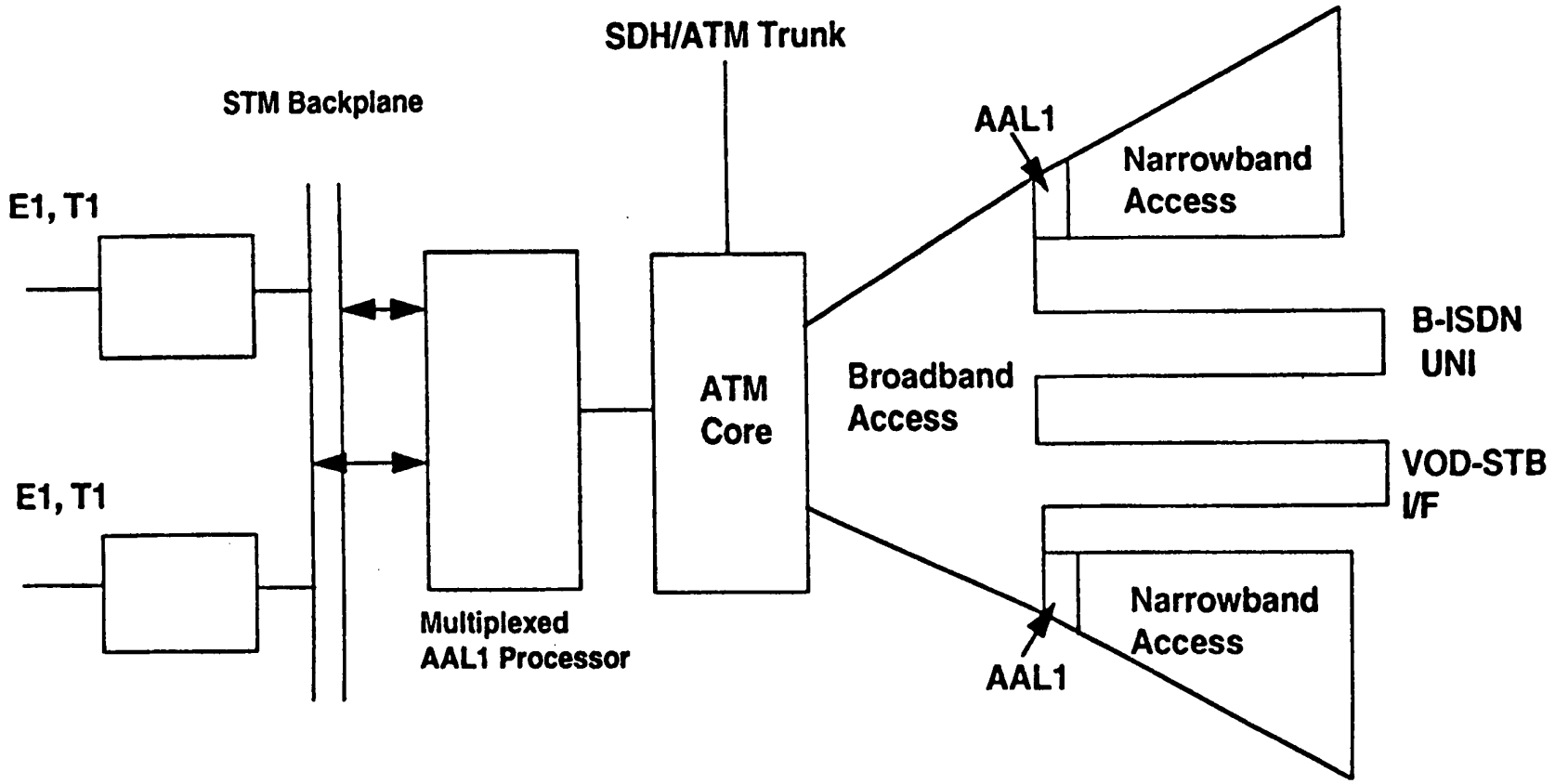


figure 2

Integrated Broadband and Narrowband Access

figure 3



for access aggregates of 6 or more channels no echo control is required

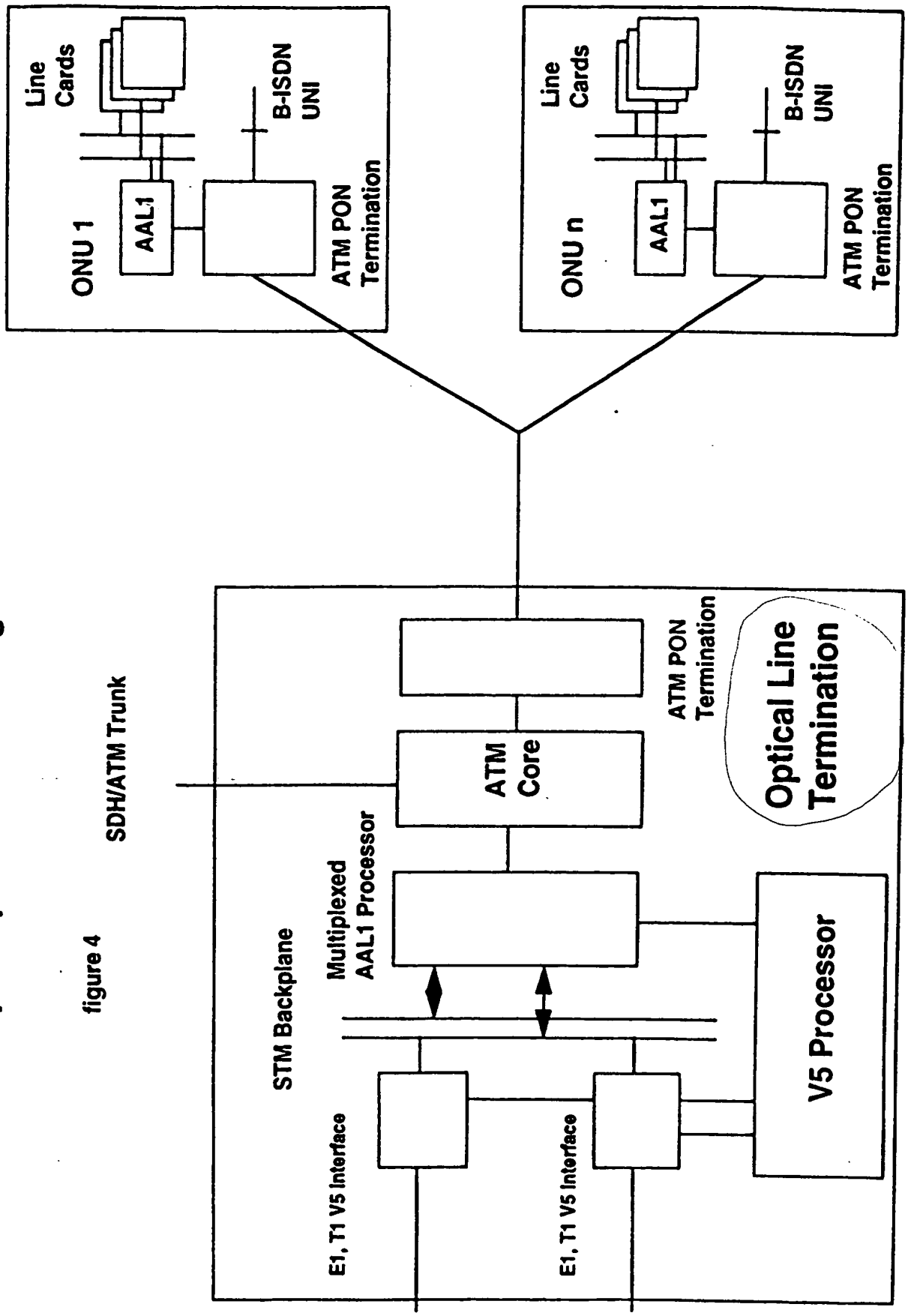


figure 4

Example Implementation using an ATM PON

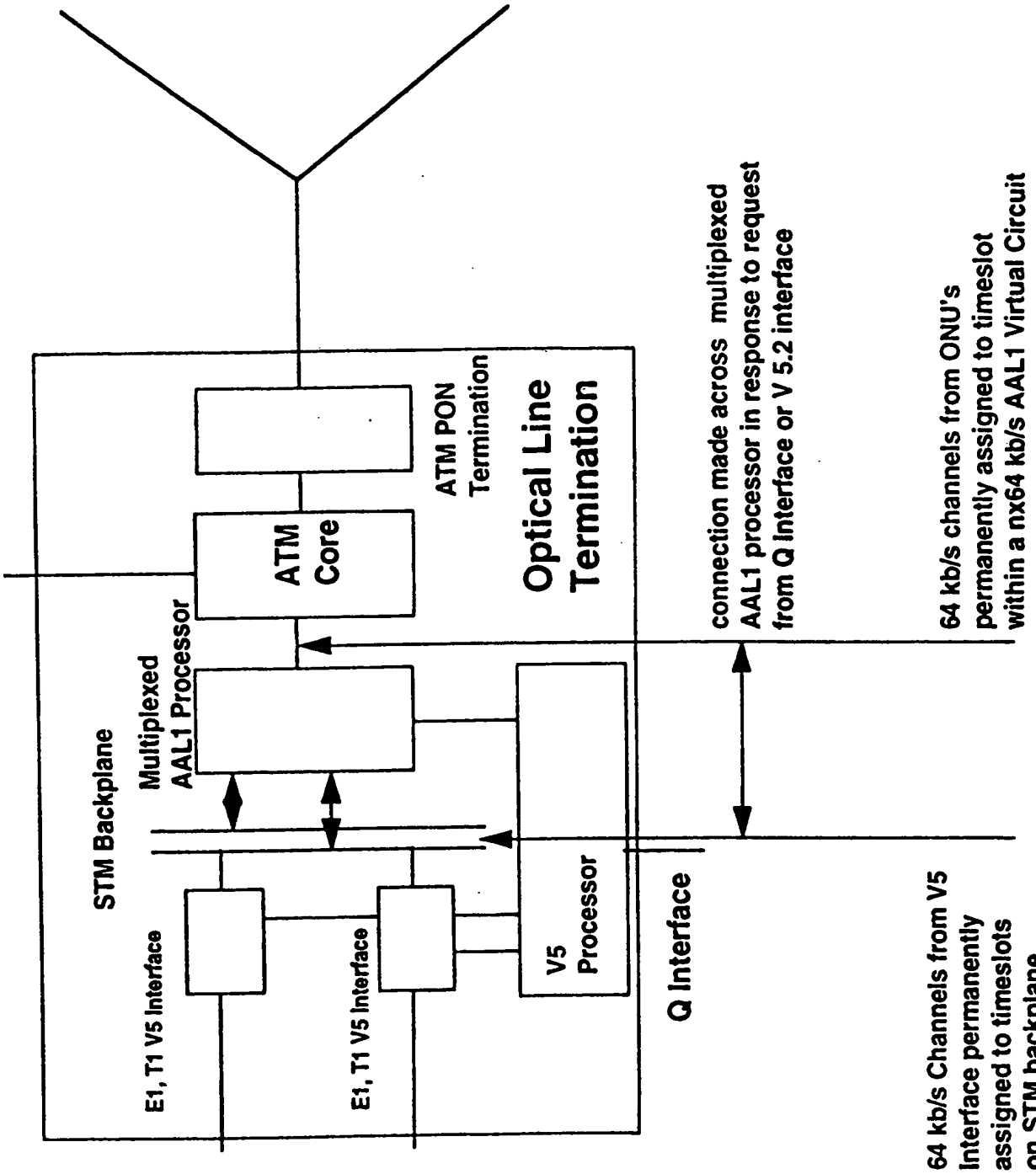

Operation of V 5.1 and V5.2
ATM PON Termination
ATM Core
Optical Line Termination
STM Backplane
Multiplexed AAL1 Processor
E1, T1 V5 Interface
E1, T1 V5 Interface
V5 Processor
Q Interface
connection made across multiplexed AAL1 processor in response to request from Q interface or V 5.2 interface
64 kb/s channels from ONU's permanently assigned to timeslot within a nx64 kb/s AAL1 Virtual Circuit
64 kb/s Channels from V5 Interface permanently assigned to timeslots on STM backplane

figure 5

INTERNATIONAL SEARCH REPORT

Intern al Application No
PCT/GB 95/01133

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04Q11/04 H04L12/64

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04Q H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO-A-92 22034 (THE TRUSTEES OF THE UNIVERSITY OF PENNSYLVANIA) 10 December 1992	1,2
A	see page 9, line 23 - page 10, line 22 see page 20, line 3 - line 6; figures 3B, 5	3-5

Y	EP-A-0 523 874 (AT&T) 20 January 1993 see column 2, line 31 - line 39 see column 2, line 58 - column 3, line 13 see column 4, line 58 - column 5, line 14 see column 9, line 1 - line 50	1,2

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[X] Further documents are listed in the continuation of box C.

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24 August 1995	01.09.95

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	INTERNATIONAL JOURNAL OF DIGITAL AND ANALOG COMMUNICATION SYSTEMS, vol. 6, no. 1, January 1993 UK, pages 3-14, ARMITAGE ET AL. ' Prototyping an ATM adaptation layer in a multimedia terminal ' see page 6, left column, line 17 - line 31 see page 9, left column, line 20 - right column, line 56; figures 1-4,6,11,13 ---	1,5
A	ICC'93, vol. 2, 23 May 1993 - 26 May 1993 GENEVA, CH, pages 873-877, XP 000371206 K. JAMES ET AL. 'TOWARDS A GLOBAL V5 INTERFACE' see page 875, right column, paragraph 2 - page 876, left column, paragraph 1; figures 5,6 ---	1
A	SPIE FIBER NETWORKS FOR VOICE, VIDEO & MULTIMEDIA SERVICE , vol. 1786, 19 November 1992 BOSTON, US, pages 48-57, XP 000444626 G. VAN DER PLAS ET AL. 'ATM over passive optical networks : system design and demonstration' see page 49, line 25 - page 50, line 7 see page 51, paragraph 2.2.2 see page 56, paragraph 3; figure 1 -----	1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Intern al Application No
PCT/GB 95/01133

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		JP-T-	6510641	24-11-94
EP-A-523874	20-01-93	AU-B-	639183	15-07-93
		AU-A-	1817792	11-03-93
		US-A-	5396494	07-03-95